intel®

SCHOTTKY BIPOLAR LSI MICROCOMPUTER SET

3212 MULTI—MODE LATCH BUFFER

The INTEL Bipolar Microcomputer Set is a family of Schottky bipolar LSI circuits which simplify the construction of microprogrammed central processors and device controllers. These processors and controllers are truly microprogrammed in the sense that their control logic is organized around a separate read-only memory called the microprogram memory. Control signals for the various processing elements are generated by the microinstructions contained in the microprogram memory. In the implementation of a typical central processor, as shown below, the microprogram interprets a higher level of instructions called macroinstructions, similar to those found in a small computer. For device controllers, the microprograms directly implement the required control functions.

The INTEL 3212 Multi-Mode Latch Buffer is a versatile 8-bit latch with three-state output buffers and built-in device select logic. It also contains an independent service request flip-flop for the generation of central processor interrupts. Because of its multi-mode capabilities, one or more 3212's can be used to implement many types of interface and support systems for Series 3000 computing elements including:

Simple data latches

Gated data buffers

Multiplexers

Bi-directional bus drivers

Interrupting input/output ports

High Performance — 50 ns Write Cycle Time

Low Input Load Current — 250 μA Maximum

Three-State Fully Buffered Outputs

High Output Drive Capability

Independent Service Request Flip-Flop

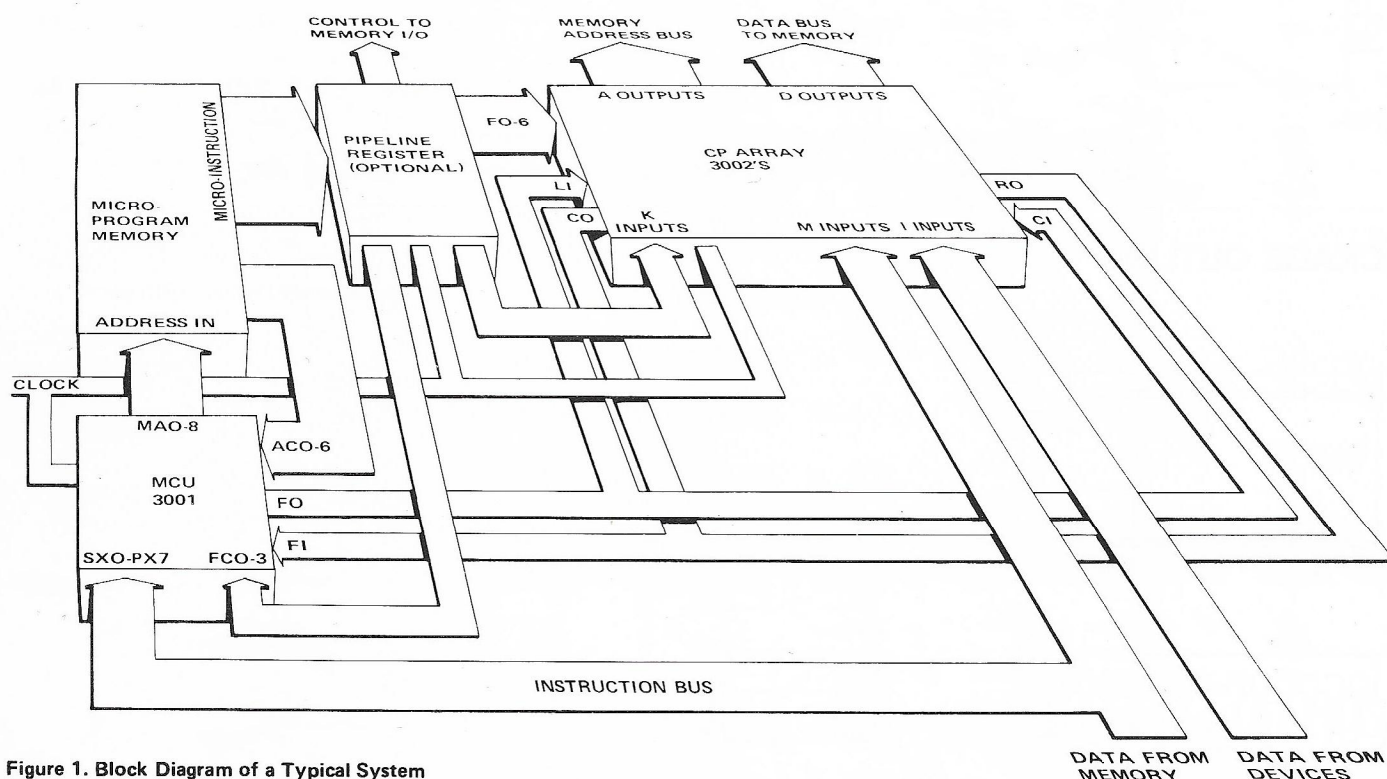Asynchronous Data Latch Clear

24 Pin DIP

Figure 1. Block Diagram of a Typical System

Other members of the INTEL Bipolar Microcomputer Set:

3001 Microprogram Control Unit	3214 Priority Interrupt Control Unit	3304A Schottky Bipolar ROM (512 x 8)
3002 Central Processing Element	3226 Inverting Bi-Directional Bus Driver	3601 Schottky Bipolar PROM (256 x 4)
3003 Look-Ahead Carry Generator	3301 Schottky Bipolar ROM (256 x 4)	3604 Schottky Bipolar PROM (512 x 8)

CONTENTS

PACKAGE CONFIGURATION

PACKAGE OUTLINE
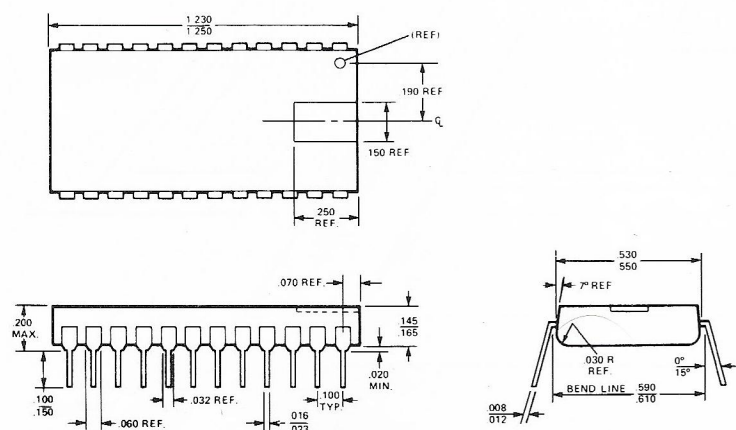
PIN DESCRIPTION

PIN	SYMBOL	NAME AND FUNCTION	TYPE[1]
1	DS_1	Device Select Input 1	active LOW
2	MD	Mode Input When MD is high (output mode) the output buffers are enabled and the write signal to the data latches is obtained from the device select logic. When MD is low (input mode) the output buffer state is determined by the device select logic and the write signal is obtained from the strobe (STB) input.	
3, 5, 7, 9, 16, 18, 20, 22	$DI_1 - DI_8$	Data Inputs The data inputs are connected to the D-inputs of the data latches.	
4, 6, 8, 10, 15, 17, 19, 21	$DO_1 - DO_8$	Data Outputs The data outputs are the buffered outputs of the eight data latches.	three-state
11	STB	Strobe Input When MD is in the LOW state, the STB input provides the clock input to the data latch.	
12	GND	Ground	
13	DS_2	Device Select Input 2 When DS_1 is low and DS_2 is high, the device is selected.	
14	CLR	Clear	active LOW
23	INT	Interrupt Output The interrupt output will be active LOW (interrupting state) when either the service request flip-flop is low or the device is selected.	active LOW

NOTE:
(1) Active HIGH, unless otherwise specified.

FUNCTIONAL DESCRIPTION

The 3212 contains eight D-type data latches, eight three-state output buffers, a separate D-type service request flip-flop, and a flexible device select/mode control section.

DATA LATCHES

The Q-output of each data latch will follow the data on its corresponding date input line (DI_1—DI_8) while its clock input is high. Data will be latched when the internal write line WR is brought low. The output of each data latch is connected to a three-state, non-inverting output buffer. The internal enable line EN is bussed to each buffer. When the EN is high, the buffers are enabled and the data in each latch is available on its corresponding data output line (DO_0—DO_8).

DEVICE SELECT LOGIC

Two input lines DS_1 and DS_2 are provided for device selection. When DS_1 is low and DS_2 is high, the 3212 is selected.

MODE CONTROL SECTION

The 3212 may be operated in two modes. When the mode input line MD is low, the device is in the input mode. In this mode, the output buffers are enabled whenever the 3212 is selected; the internal WR line follows the STB input line.

When MD is high, the device is in the output mode and, as a result, the output buffers are enabled. In this mode, the write signal for the data latch is obtained from the device select logic.

SERVICE REQUEST FLIP-FLOP AND STROBE

The service request flip-flop SR is used to generate and control central processor interrupt signals. For system reset, the SR flip-flop is placed in the non-interrupting state (i.e., SR is set) by bringing the CLR line low. This simultaneously clears (resets) the 8-bit data latch.

The Q output of the SR flip-flop is logically ORed with the output of device select logic and then inverted to provide the interrupt output INT. The 3212 is considered to be in the interrupting state when the INT output is low. This allows direct connection to the active LOW priority request inputs of the INTEL 3214 Interrupt Control Unit.
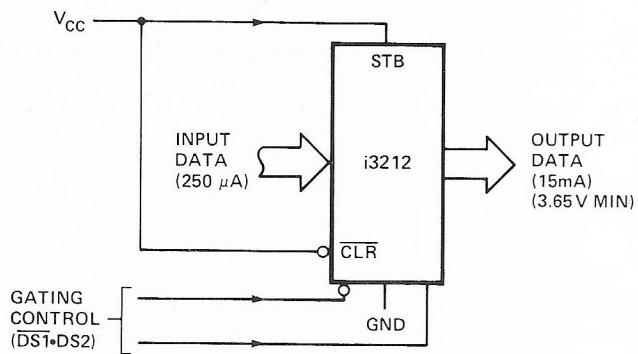
When operated in the input mode (i.e., MD low) the strobe input STB is used to synchronously write data into the data latch and place the SR flip-flop in the interrupting (reset) state. The interrupt is removed by the central processor when the interrupting 3212 is selected.
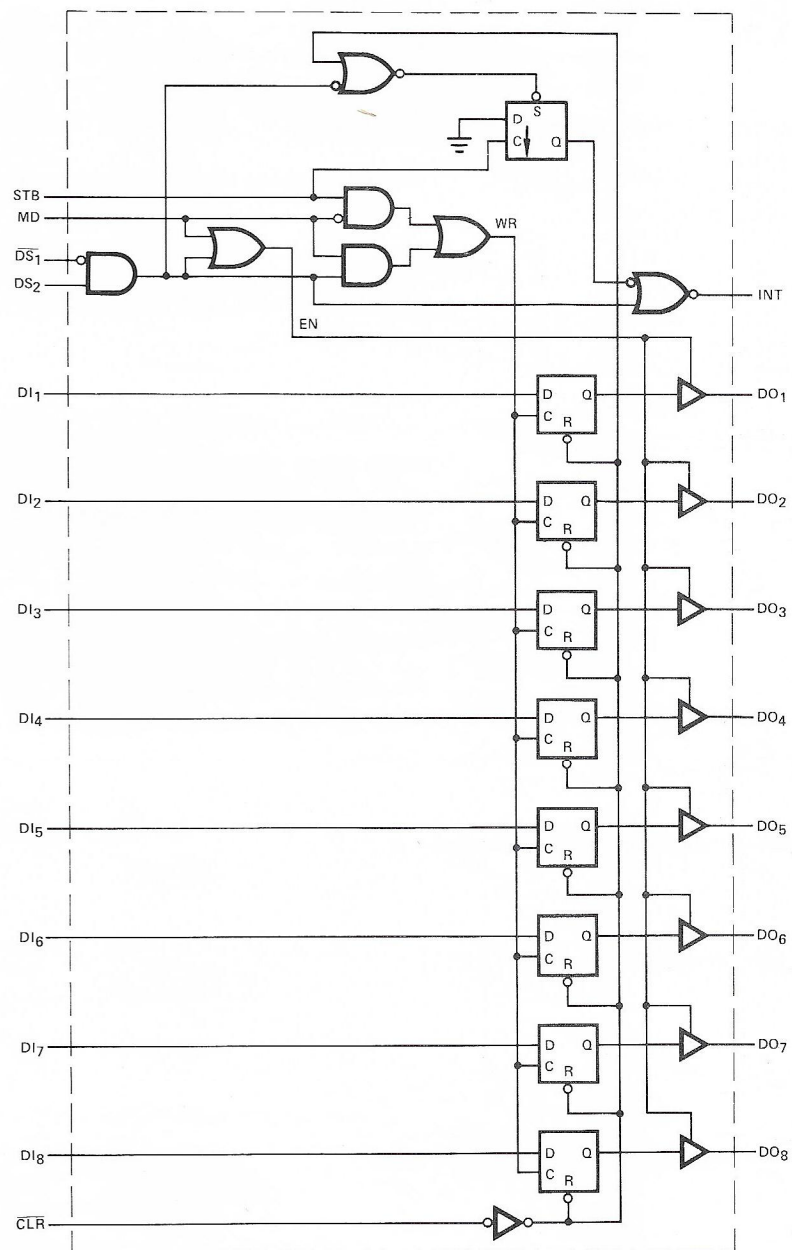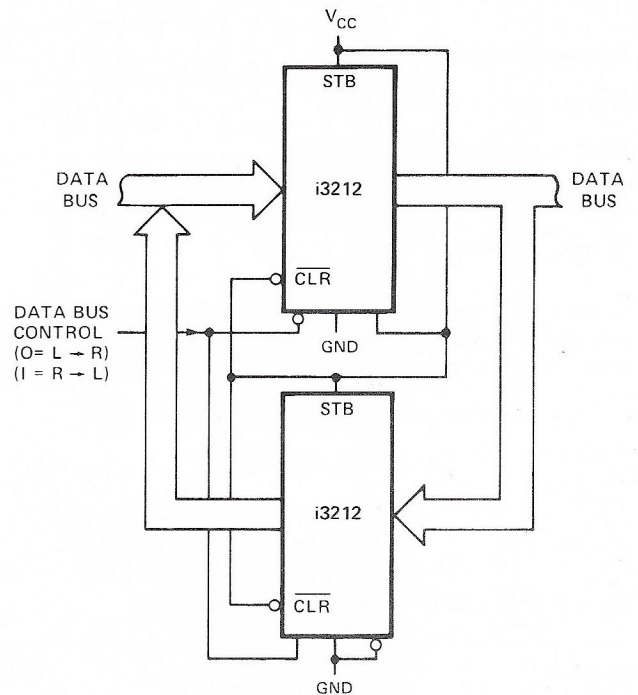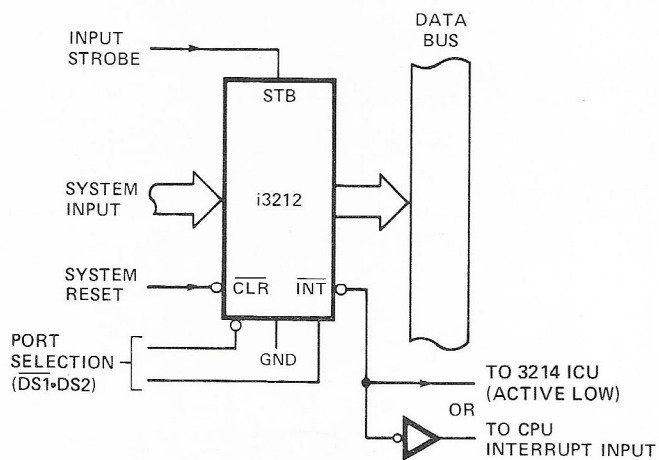

3212 Logic Diagram

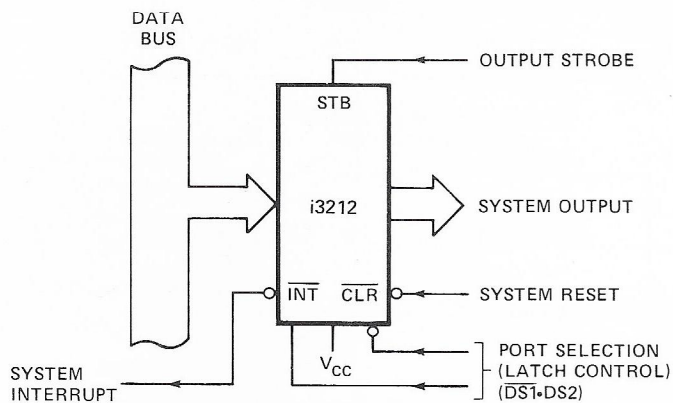# TYPICAL CONFIGURATIONS

GATED BUFFER (TRI-STATE)

BI-DIRECTIONAL BUS DRIVER

INTERRUPTING INPUT PORT

OUTPUT PORT (WITH HAND-SHAKING)

D.C. AND OPERATING CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias . . . . .0°C to 70°C

Storage Temperature . . . . –65°C to +160°C

All Output and Supply Voltages . . . . –0.5V to +7V

All Input Voltages . . . .–1.0V to +5.5V

Output Currents . . . . 100 mA

*COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

$T_A = 0°C$ to $+75°C$ $V_{CC} = +5V \pm 5\%$

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
I_F	Input Load Current STB, DS_2, CLR, DI_1-DI_8 Inputs			–.25	mA	$V_F = .45V$
I_F	Input Load Current MD Input			–.75	mA	$V_F = .45V$
I_F	Input Load Current DS_1 Input			–1.0	mA	$V_F = .45V$
I_R	Input Leakage Current STB, DS, CLR, DI_1-DI_8 Inputs			10	μA	$V_R = 5.25V$
I_R	Input Leakage Current MD Input			30	μA	$V_R = 5.25V$
I_R	Input Leakage Current DS_1 Input			40	μA	$V_R = 5.25V$
V_C	Input Forward Voltage Clamp			–1	V	$I_C = -5$ mA
V_{IL}	Input "Low" Voltage			.85	V	
V_{IH}	Input "High" Voltage	2.0			V	
V_{OL}	Output "Low" Voltage			.45	V	$I_{OL} = 15$ mA
V_{OH}	Output "High" Voltage	3.65	4.0		V	$I_{OH} = -1$ mA
I_{SC}	Short Circuit Output Current	–20		–65	mA	$V_O = 0V$
$|I_O|$	Output Leakage Current High Impedance State			100	μA	$V_O = .45V/5.25V$
I_{CC}	Power Supply Current		90	130	mA	

6

A.C. CHARACTERISTICS

| Symbol	Parameter	Min.	Typ.	Max.	Unit	
t_{PW}	Pulse Width	25			ns	
t_{PD}	Data To Output Delay			25	ns	
t_{WE}	Write Enable To Output Delay			40	ns	
t_{SET}	Data Setup Time	15			ns	
t_H	Data Hold Time	20			ns	
t_R	Reset To Output Delay			40	ns	
t_S	Set To Output Delay			30	ns	
t_E	Output Enable Time			40	ns	C_L = 30 pf
t_D	Output Disable Time			30	ns	C_L = 5 pf
t_C	Clear To Output Display			45	ns	

TEST CONDITIONS:

Input pulse amplitude of 2.5 volts.
Input rise and fall times of 5 ns between 1 volt and 2 volts.
Output load of 15 mA and 30 pF.
Speed measurements are taken at the 1.5 volt level.
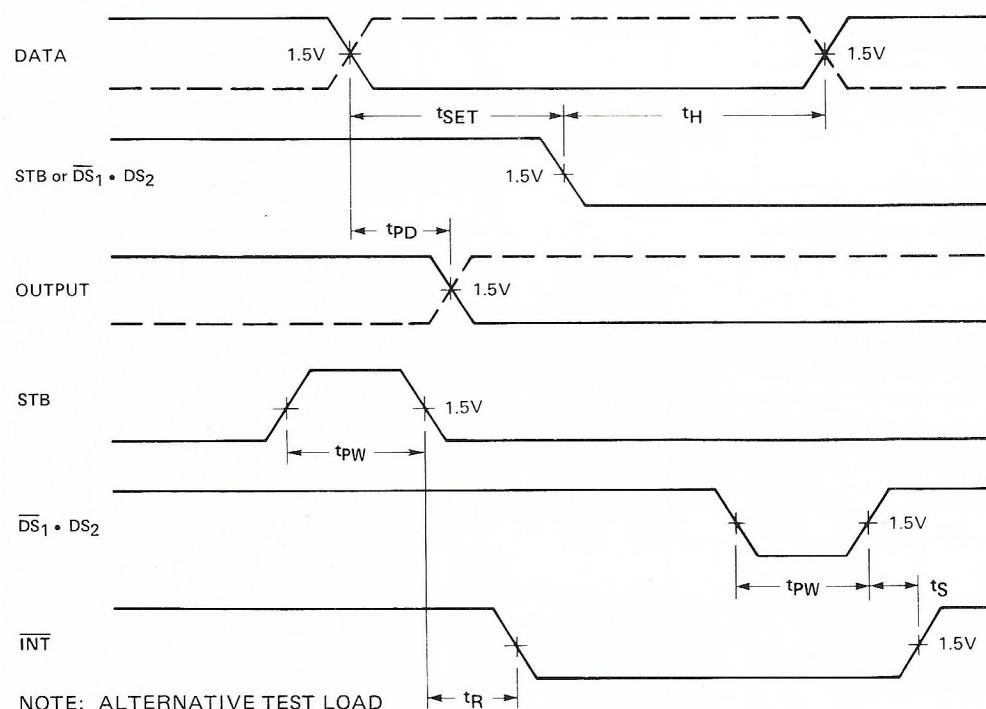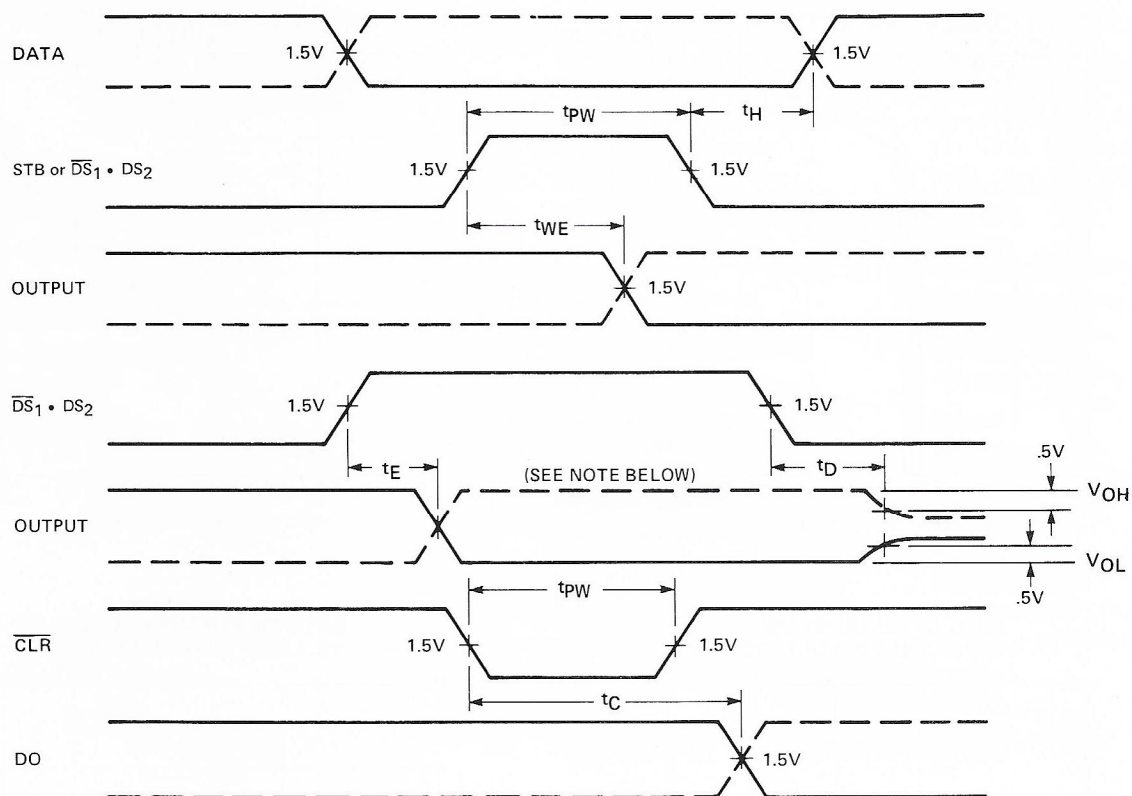
TEST LOAD CIRCUIT:
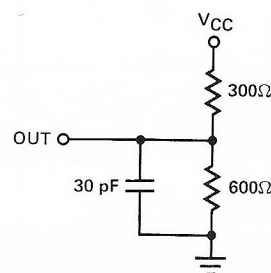
CAPACITANCE[1]

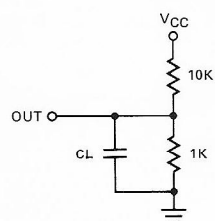| Symbol	Test	LIMITS			
		Min.	Typ.	Max.	Units
C_{IN}	DS_1, MD Input Capacitance		9	12	pf
C_{IN}	DS_2, CLR, STB, DI_1–DI_8 Input Capacitance		5	9	pf
C_{OUT}	DO_1–DO_8 Output Capacitance		8	12	pf

NOTE:
(1) This parameter is periodically sampled and is not 100% tested. Condition of measurement is f = 1 MHz, V_{BIAS} = 2.5V, V_{CC} = 5V and T_A = 25°C.

WAVEFORMS

DATA ⟶ 1.5V

STB or $\overline{DS}_1 \cdot DS_2$ ⟶ 1.5V — t_{PW} — t_H

1.5V

OUTPUT — t_{WE} — 1.5V

$\overline{DS}_1 \cdot DS_2$ ⟶ 1.5V ⟶ 1.5V

t_E (SEE NOTE BELOW) t_D .5V V_{OH}

OUTPUT V_{OL}

t_{PW} .5V

$\overline{CLR}$ ⟶ 1.5V ⟶ 1.5V

t_C

DO ⟶ 1.5V

DATA ⟶ 1.5V ⟶ 1.5V

t_{SET} t_H

STB or $\overline{DS}_1 \cdot DS_2$ ⟶ 1.5V

t_{PD}

OUTPUT ⟶ 1.5V

STB ⟶ 1.5V

t_{PW}

$\overline{DS}_1 \cdot DS_2$ ⟶ 1.5V

t_{PW} t_S

$\overline{INT}$ ⟶ 1.5V

NOTE: ALTERNATIVE TEST LOAD — t_R
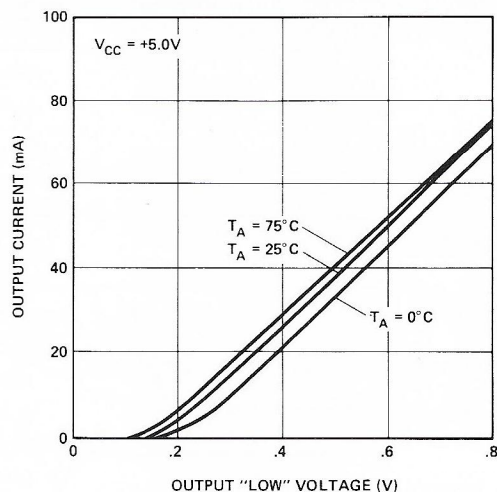
V_{CC}

10K

OUT

C_L 1K
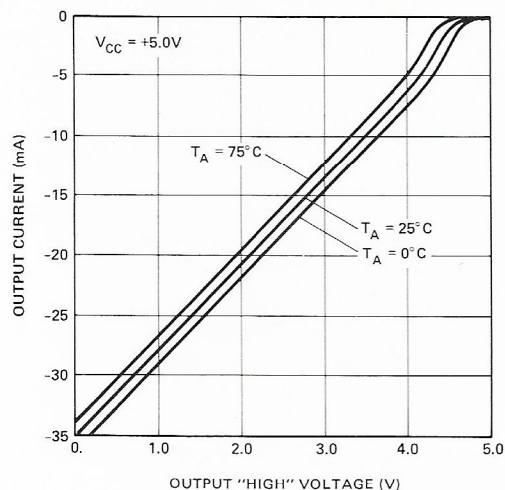
8

TYPICAL A.C. AND D.C. CHARACTERISTICS

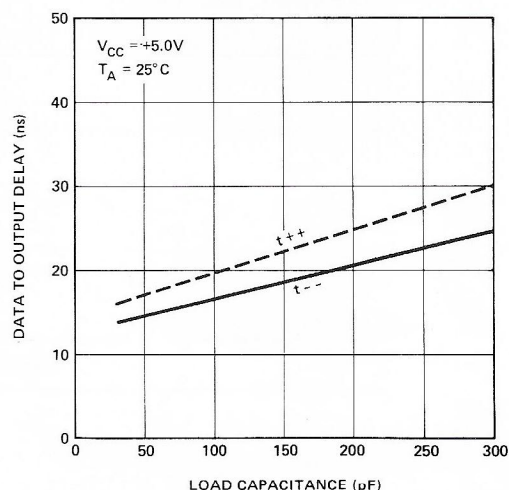### INPUT CURRENT VS. INPUT VOLTAGE
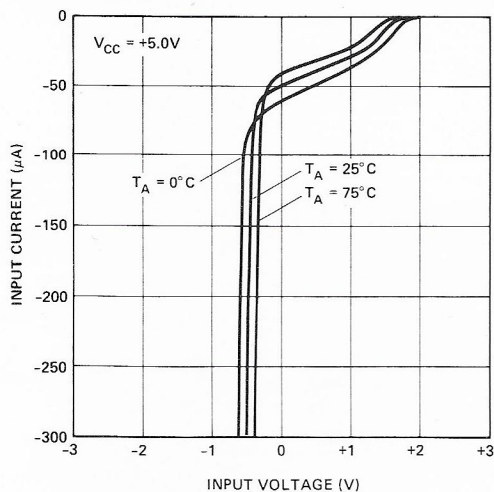
OUTPUT CURRENT VS. OUTPUT "LOW" VOLTAGE
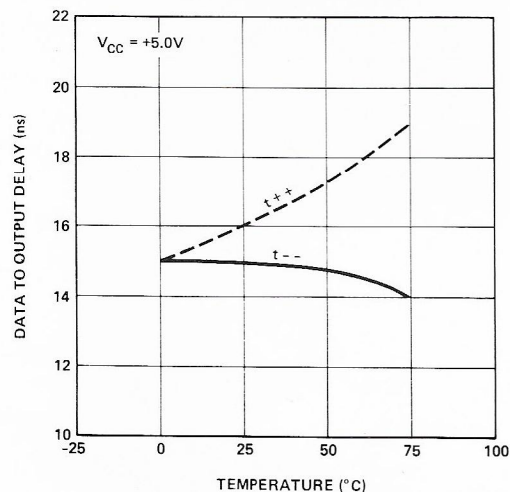

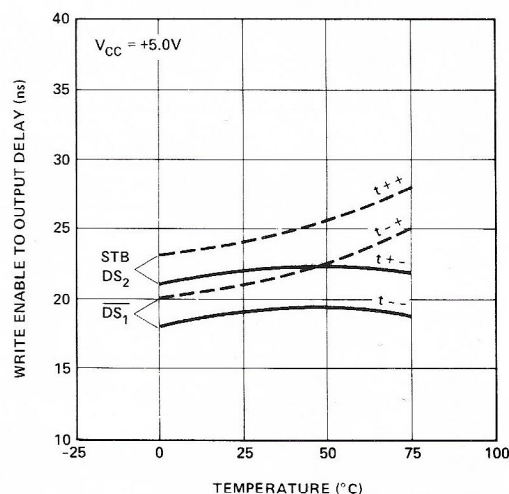### OUTPUT CURRENT VS. OUTPUT "HIGH" VOLTAGE

DATA TO OUTPUT DELAY VS. LOAD CAPACITANCE

DATA TO OUTPUT DELAY VS. TEMPERATURE

WRITE ENABLE TO OUTPUT DELAY VS. TEMPERATURE

ORDERING INFORMATION

Part Number	Description
P3212	Multi-Mode Latch Buffer

intel®

Intel Corporation
3065 Bowers Avenue
Santa Clara, California 95051
Tel: (408) 246-7501
TWX: 910-338-0026
Telex: 34-6372

WESTERN
1651 East 4th Street
Suite 228
Santa Ana, California 92701
Tel: (714) 835-9642
TWX: 910-595-1114

MID-AMERICA
6350 L.B.J. Freeway
Suite 178
Dallas, Texas 75240
Tel: (214) 661-8829
TWX: 910-860-5487

GREAT LAKES REGION
8312 North Main Street
Dayton, Ohio 45415
Tel: (513) 890-5350
TELEX: 288-004

EASTERN
2 Militia Drive
Suite 4
Lexington, Massachusetts 02173
Tel: (617) 861-1136
TWX: 710-321-0187

MID-ATLANTIC
520 Pennsylvania Avenue
Suite 102
Fort Washington, Pennsylvania 19034
Tel: (215) 542-9444
TWX: 510-661-3055

EUROPE
Belgium
Intel Office
216 Avenue Louise
Brussels B1050
Tel: 649-20-03
TELEX: 24814

ORIENT
Japan
Intel Japan Corporation
Kasahara Bldg.
1-6-10, Uchikanda
Chiyoda-ku
Tokyo 101
Tel: (03) 295-5441
TELEX: 781-28426